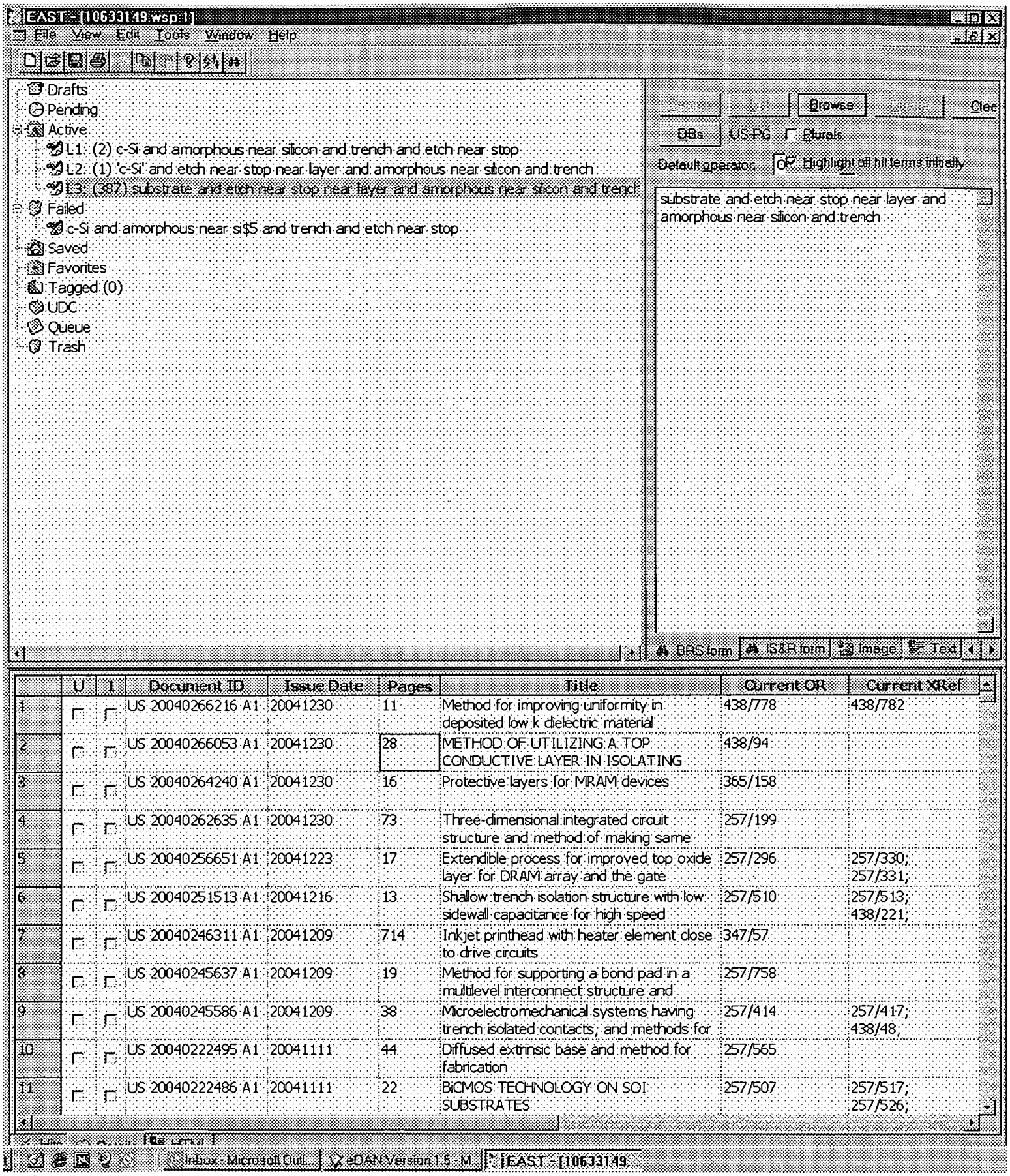
EAST - [10633149.wsp]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (2) c-Si and amorphous near silicon and trench and etch near stop
L2: (1) 'c-Si' and etch near stop near layer and amorphous near silicon and trench
L3: (387) substrate and etch near stop near layer and amorphous near silicon and trench
Failed
c-Si and amorphous near si$5 and trench and etch near stop
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Browse
Clear
DBs
US-PG
Plurals
Default operator:
Highlight all hit terms initially
substrate and etch near stop near layer and amorphous near silicon and trench
BRS form
IS&R form
Image
Text
U
I
Document ID
Issue Date
Pages
Title
Current OR
Current XRef
1 US 20040266216 A1 20041230 11 Method for improving uniformity in deposited low k dielectric material 438/778 438/782
2 US 20040266053 A1 20041230 28 METHOD OF UTILIZING A TOP CONDUCTIVE LAYER IN ISOLATING 438/94
3 US 20040264240 A1 20041230 16 Protective layers for MRAM devices 365/158
4 US 20040262635 A1 20041230 73 Three-dimensional integrated circuit structure and method of making same 257/199
5 US 20040256651 A1 20041223 17 Extendible process for improved top oxide layer for DRAM array and the gate 257/296 257/330; 257/331;
6 US 20040251513 A1 20041216 13 Shallow trench isolation structure with low sidewall capacitance for high speed 257/510 257/513; 438/221;
7 US 20040246311 A1 20041209 714 Inkjet printhead with heater element close to drive circuits 347/57
8 US 20040245637 A1 20041209 19 Method for supporting a bond pad in a multilevel interconnect structure and 257/758
9 US 20040245586 A1 20041209 38 Microelectromechanical systems having trench isolated contacts, and methods for 257/414 257/417; 438/48;
10 US 20040222495 A1 20041111 44 Diffused extrinsic base and method for fabrication 257/565
11 US 20040222486 A1 20041111 22 BiCMOS TECHNOLOGY ON SOI SUBSTRATES 257/507 257/517; 257/526;
Inbox - Microsoft Out...
eDAN Version 1.5 - M...
EAST - [10633149...